Academic Program: PG

Academic Year 2021-22

Department of Electronics and Communication Engineering

M. Tech in Digital Electronics

III & IV Semester Syllabus

SHRI DHARMASTHALA MANJUNATHESHWARA COLLEGE OF

ENGINEERING & TECHNOLOGY,

DHARWAD – 580 002

(An Autonomous Institution Approved by AICTE & Affiliated to VTU, Belagavi)

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SDM College of Engineering & Technology, Dharwad

It is certified that the scheme and syllabus for III & IV semester M.Tech in Digital Electronics is recommended by the Board of Studies of Electronics and Communication Engineering Department and approved by the Academic Council, SDM College of Engineering & Technology, Dharwad. This scheme and syllabus will be in force from the academic year 2021-22 till further revision.

Chairman BOS & HOD Principal

SDM College of Engineering & Technology, Dharwad-02

Department of Electronics & Communication Engineering

College - Vision and Mission

VISION:

To develop competent professionals with human values.

MISSION:

1. To have contextually relevant Curricula.
2. To promote effective Teaching Learning Practices supported by Modern Educational Tools and Techniques.
3. To enhance Research Culture.
4. To involve Industrial Expertise for connecting classroom content to real life situations.
5. To inculcate Ethics and impart soft-skills leading to overall Personality Development.

SDMCET- Quality Policy

- In its quest to be a role model institution, committed to meet or exceed the utmost interest of all the stake holders.

SDMCET- Core Values

- Competency
- Commitment
- Equity
- Team work and
- Trust

Department - Vision and Mission

VISION:

Fostering excellence in the field of Electronics & Communication Engineering, showcasing innovation, research and performance with continuous Industry – Institute Interaction with the blend of Human values.

MISSION:

M1: To provide quality education in the domain of Electronics & Communication Engineering through state of the art curriculum, **effective teaching learning** process and the best of laboratory facilities.

M2: To encourage **innovation**, **research** culture and **team work** among students.

M3: **Interact and work** closely with **industries** and **research organizations** to accomplish knowledge at par.

M4: To train the students for attaining **leadership with ethical values** in developing and applying technology for the **betterment of society** and sustaining the global environment.

Program Educational Objectives (PEOs):

1. To equip the students with sound technical knowledge and capability of keeping in pace with changing technology.

2. To develop self confidence for independent working, leadership quality and spirit to work cohesively with group.

3. To inculcate research orientation in the aspect of system design.

4. To imbibe professional and social ethics and to bring awareness regarding societal responsibility, moral and safety related issues.

Program Outcomes (POs):

PO1: An ability to independently carry out research / investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor program.

PO4: Apply the knowledge of engineering and state of the art technology to solve complex engineering problems.

PO5: An ability to identify, formulate and design technically and socially relevant digital electronics systems or processes to meet desired needs within realistic constraints.

PO6: Apply professional ethics and engage in independent and life long learning in the broadest context of technological changes.

Scheme for III Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
20PDEC300	VLSI for Signal Processing	4-0-0	4	50	100	3		
20PDEE35X	Elective 5	3-0-0	3	50	100	3		
20PDEE35X	Elective 6	3-0-0	3	50	100	3		
20PDEE35X	Elective 7	3-0-0	3	50	100	3	--	--
OR								
20PDEL300	**Internship in Industry or R&D organization	Min 4 weeks during vacation after 2nd sem	3	50	--	--	100	3
20PDEL301	***Project Phase-I	0-0-15	9	50			50	3
Total		**13-0-15 /10-4 weeks-15)**	**22**	**250**	**400/ 300**		**50/150**	

20PDEE350	Advances in VLSI Design
20PDEE351	System on Chip Design
20PDEE352	Cryptographic Systems
20PDEE353	Image and Video Processing
20PDEE354	Modern DSP
20PDEE355	Wireless Sensor Networks
20PDEE356	Advanced FPGA Design
20PDEE357	MEMS

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

***SEE** for theory courses is conducted for 100 marks and reduced to 50 marks.

**** Internship: The students are expected to undergo training in industry for a period of ***four weeks*** during the vacation immediately after completion of II Semester examination. A faculty is to be allotted to guide the student. A committee consisting of three faculty members shall evaluate the work carried out and the knowledge the students have acquired. **OR The students can take one elective course if they do not undergo internship.**

*****Project phase-I: The students are expected to formulate the problem and carry out the intensive literature survey along with preliminary investigations supporting the project phase-II in IV semester.

Scheme for IV Semester

Course Code	Course Title	Teaching		Examination				
		L-T-P (Hrs/ Week)	Credits	CIE	Theory (SEE)		Practical (SEE)	
				Max. Marks	*Max. Marks	Duration in hours	Max. Marks	Duration in hours
20PDEL400	Project Phase-II	0-0-20	22	100	--	--	100	3
Total		**0-0-20**	**22**	**100**	**--**	**--**	**100**	

CIE: Continuous Internal Evaluation **SEE**: Semester End Examination

L: Lecture **T**: Tutorials **P**: Practical

Project Phase-II: The students are expected to work on a project for the full semester in an industry or an institution

Total Credits offered for the first year: 44

Total Credits offered for the Second year: 44

III Semester

20PDEC300	VLSI for Signal Processing	(4-0-0) 4

Contact Hours: 52

Course Learning Objectives (CLOs):

The subject focuses on several high level architectural transformations that can be used to design families of architectures for a given algorithm and develop knowledge of the central ideas of implementation of DSP algorithm with optimized hardware.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** high-level architectural transformation for effective integrated circuit implementations	4	3	6
CO-2	**Analyze** high-level algorithmic transformation for effective integrated circuit implementations	4	3	6
CO-3	**Explain and apply** arithmetic strength reduction techniques	5	3	-
CO-4	**Explain and apply** numerical strength reduction techniques	5	3	-
CO-5	**Compare** the techniques of reducing the computational complexity	4	-	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	3	3	1

Pre-requisites: Digital Signal Processing, VLSI design

Contents:

1) **Introduction to Parallel Processing:** Parallelism in uniprocessor systems, Parallel Computer structures, architectural classification schemes, Parallel Processing Applications. Principles of Pipelining and Array Processors, an overlapped parallelism, instruction and arithmetic pipelines, data buffering and busing structures, SIMD array processors, parallel algorithm for array Processors. **08 Hrs**

2) **Iteration Bound, Pipelining, Parallel Processing, Retiming**: Introduction, Data-Flow graph representations, Loop Bound and Iteration Bound, Algorithms for computing iteration bound, Pipelining of FIR Digital Filters, Parallel Processing, Pipelining and Parallel Processing for low power, Retiming Definitions and properties, solving systems of inequalities, Retiming Techniques. **09 Hrs**
3) **Unfolding and Folding**: Introduction, An algorithm for unfolding, properties of unfolding, critical path, unfolding and retiming, Applications of unfolding, folding transformation, register minimization techniques, register minimization in folded architectures, folding of multi-rate systems. **08 Hrs**
4) **Algorithmic Strength Reduction in filters and Transforms:** Introduction, Parallel FIR filters, Discrete Cosine Transform and Inverse Discrete Cosine Transform, parallel architectures for Rank-Order filters. **09 Hrs**
5) **Pipelined and Parallel Recursive filters**: Introduction, pipeline interleaving in digital filters, pipelining in 1^{st}order IIR digital filters, parallel processing for IIR filters, combined pipelining and parallel processing for IIR filters, low-power IIR Filter Design using pipelining and parallel processing. **09 Hrs**
6) **Redundant Arithmetic and Numerical Strength Reduction:** Introduction, Redundant number representations, carry-free radix-2 addition and subtraction, hybrid radix-4 addition, radix-2 hybrid redundant multiplication architectures, data format conversion, sub-expression elimination, multiple constant multiplication, sub-expression sharing in digital filters, additive and multiplicative number splitting. **09 Hrs**

Reference Books:

1) Kai Hwang & Faye A. Briggs, “Computer Architecture and Parallel Processing” McGraw-Hill Series, 1984.
2) Parhi, K.K., “VLSI Digital Signal Processing Systems: Design and Implementation”, John Wiley, 2007.
3) Wanhammar, L., “DSP Integrated Circuits”, Academic Press, 1999.
4) Magdy A. Bayoumi, “VLSI Design Methodologies for Architectures”, Kluwer Academic Publishers, 1994.
5) Mitra, S.K., “Digital Signal Processing: A Computer Based Approach”, McGraw Hill, 2007, 3rd edition.

20PDEE350	Advances in VLSI Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the theory and design principles of VLSI devices and circuits. The course concentrates on the study and analysis of various combinational and sequential MOS logic circuits for VLSI applications.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Explain** the theory, construction, characteristics and various processes involved in the CMOS technology.	-	-	4
CO-2	**Discuss** the construction and working of MESFETS, MIS structures and MODFETS.	-	4	-
CO-3	**Apply** rules involved in the schematic and layout design for VLSI circuits.	4	5,6	2
CO-4	**Explain** CMOS circuits with respect to different technologies.	-	4,5	-
CO-5	**Identify and describe** the challenges involved in digital CMOS VLSI design.	-	3,4	5,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	-	1	2	2	1.6	1.5

Pre-requisites: Analog Electronics, Network Analysis, Digital Circuits.

Contents:

1) **Review of MOS Circuits:** MOS and CMOS static plots, switches, comparison between CMOS and Bi - CMOS. **4 Hrs**
2) **MESFETS:** MESFET and MODFET operations, quantitative description of MESFETS. **5 Hrs**
3) **MIS Structures and MOSFETS:** MIS systems in equilibrium, under bias, small signal operation of MESFETS and MOSFETS. **5 Hrs**

4) **Super Buffers, Bi-CMOS and Steering Logic:** Introduction, RC delay lines, super buffers- An NMOS super buffer, tri state super buffer and pad drivers, CMOS super buffers, Dynamic ratio less inverters, large capacitive loads, pass logic, designing of transistor logic, General functional blocks–NMOS and CMOS functional blocks. **8 Hrs**
5) **Special Circuit Layouts Technology Mapping:** Introduction, Talley circuits, NAND-NAND, NOR-NOR, and AOI Logic, NMOS, CMOS Multiplexers, Barrel shifter, Wire routing and module layout. **9 Hrs**
6) **System Design:** CMOS design methods, structured design methods, Strategies encompassing hierarchy, regularity, modularity & locality, CMOS Chip design Options, programmable logic, Programmable inter connect, programmable structure, Gate arrays standard cell approach, Full custom design. Beyond CMOS. **8 Hrs**

Reference Books:

1) Kevin F. Brennan, "Introduction to Semiconductor Device", Cambridge University publications, 2005.
2) Eugene D. Fabricius, "Introduction to VLSI Design", McGraw-Hill International publications,1990.
3) D. A. Pucknell, "Basic VLSI Design", PHI Publication, 2001.
4) Wayne Wolf, "Modern VLSI Design" Pearson Education, Second Edition, 2002.

20PDEE351 System On Chip Design (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on to provide an appreciation for the motivation behind SoC design, the challenges of SoC design, and the overall SoC design flow.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** the basics of CMOS and SOC	-	1	3
CO-2	**Analysis** of circuits with equations for performance Maximization	-	4	5
CO-3	**Modeling** of Design flow with	1	3	2

	types of SOC with timing issues and verification			
CO-4	**Design** of cache memory, Flash memory with MESI protocol	1	4	3
CO-5	**Evaluate** Mp SOC's, Bus architectures and NoC architectures case studies	-	3,4	5,6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.7	1	1.5	2	1	1

Pre-requisites: Analog Electronics, Engineering Mathematics, CMOS VLSI Design

Contents:

1) **Motivation for SoC Design:** Review of Moore's law and CMOS scaling, benefits of system-on-chip integration in terms of cost, power, and performance. Comparison on System-on-Board, System-on-Chip, and System-in-Package. Typical goals in SoC design – cost reduction, power reduction, design effort reduction, performance maximization. Productivity gap issues and the ways to improve the gap – IP based design and design reuse. **10 Hrs**
2) **System On Chip Design Process:** A canonical SoC Design, SoC Design flow, waterfall vs spiral, top down vs bottom up, Specification requirement, Types of Specification, System Design Process, System level design issues, Soft IP vs Hard IP, IP verification and Integration, Hardware-Software codesign, Design for timing closure, Logic design issues, Verification strategy, On chip buses and interfaces, Low Power, Hardware Accelerators in Soc. **10 Hrs**
3) **Embedded Memories:** cache memories, flash memories, embedded DRAM. Topics related to cache memories. Cache coherence. MESI protocol and Directory-based coherence **10 Hrs**
4) **Interconnect architectures for SoC:** Bus architecture and its limitations. Network on Chip (NOC) topologies. Mesh-based NoC. Routing in an NoC. Packet switching and wormhole routing **09 Hrs**

Reference Books:

1) Sudeep Pasricha and Nikil Dutt, "On-Chip Communication Architectures: System on Chip Interconnect", Morgan Kaufmann Publishers © 2008.
2) Rao R. Tummala, Madhavan Swaminathan, "Introduction to system on package sop- Miniaturization of the Entire System", McGraw-Hill, 2008.
3) James K. Peckol, "Embedded Systems: A Contemporary Design Tool", Wiley Student Edition.

4) Michael Keating, Pierre Bricaud, “Reuse Methodology Manual for System on Chip designs”, Kluwer Accademic Publishers, 2nd edition, 2008.

5) Sung-Mo Kang, Yusuf Leblebici, “CMOS Digital Integrated Circuits”, Tata Mcgraw-Hill, 3rd Edition.

20PDEE352	Cryptographic Systems	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on techniques of enciphering and deciphering messages to maintain privacy of confidential data. It also discusses algorithms for authentication and integrity.

Course Outcomes (COs):

Description of Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze** and **Apply** different symmetric cryptographic techniques to encrypt and decrypt data.	-	4,5	1,3
CO-2	**Describe** basic mathematical concepts and pseudorandom number generators required for cryptography.	4	-	3
CO-3	**Apply** and **estimate** different asymmetric cryptographic algorithms.	5	1	6
CO-4	**Explain** authentication functions to authenticate and protect the encrypted data.	5	-	6
CO-5	**Analyze** key exchange algorithms.	-	1	3
CO-6	**Discuss** algorithms for digital signature schemes.	-	4,5	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.5	-	1	2.33	2.5	1

Pre-requisites: Communication networks and finite fields

Contents:

1) **Symmetric Block Ciphers**: Terminology, Traditional Block Cipher structure, Data encryption standard (DES), Double DES, 3DES, The AES Cipher.

Number Theory: Introduction to modular arithmetic, Prime Numbers, Fermat's and Euler's theorem, primality testing, Discrete logarithms. **11 Hrs**

2) **Public-Key Cryptosystems**: Principles, The RSA algorithm, Diffie- Hellman Key Exchange, Elgamal cryptographic system, Elliptic Curve Arithmetic, Elliptic Curve Cryptography. **09 Hrs**
3) **Pseudo-Random-Sequence Generators and Stream Ciphers:** Linear Congruential Generators, Linear Feedback Shift Registers, Design and analysis of stream ciphers, Stream ciphers using LFSRs, A5, Hughes XPD/KPD, Additive generators, GIFFORD, Algorithm M. **07 Hrs**
4) **One-Way Hash Functions:** Background, SNEFRU, N-Hash, MD5, Secure Hash Algorithm [SHA], Message Authentication Codes. **06 Hrs**
5) **Digital Signatures:** Digital signatures, Elgamal Digital Signature Scheme, Digital signature Algorithm, RSA digital signatures, Elliptic Curve DSA. **06 Hrs**

Reference Books:

1) William Stallings, "Cryptography and Network Security Principles and Practice", Pearson Education Inc., 6th Edition, 2014, ISBN:978-93-325-1877-3.
2) Bruce Schneier, "Applied Cryptography Protocols, Algorithms, and Source code in C", Wiley Publications, 2nd Edition, ISBN: 9971-51-348-X.
3) Behrouz A. Forouzan, "Cryptography and Network Security", 2nd Edition, TMH, 2007.
4) AtulKahate, "Cryptography and Network Security", 3rd Edition, TMH, 2013.

20PDEE353 Image and Video Processing (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on image sampling, quantization, various image enhancement techniques, color image processing, image compression and fundamental concepts in video processing. The course also discusses various applications of image processing.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to PO (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Describe** image sampling, quantization and model of color vision.	-	-	2

CO-2	**Apply** suitable image enhancement and restoration techniques.	-	4, 3	2
CO-3	**Differentiate** various filtering techniques in image processing.	-	3	2,1
CO-4	**Choose** appropriate feature extraction technique in analyzing the given image.	3	4	1
CO-5	**Select** appropriate image reconstruction algorithms and video processing techniques.	3	2	1

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.0	1.25	2.5	2.0	-	-

Pre-requisites: Digital signal processing**,** Stochastic and random process.

Contents:

1) **Image Perception:** Light, Luminance, Brightness, Contrast, MTF of the visual system, Visibility function, Monochrome vision models, Fidelity criteria, Color representation, Chromaticity diagram, Color coordinate systems, Color difference measures, Color vision model, Temporal properties of vision. **04 Hrs**
2) **Image Sampling and Quantization:** Introduction, 2D sampling theory, Limitations in sampling & reconstruction, Quantization, Optimal quantizer, Compander, Visual quantization. **05 Hrs**
3) **Image Enhancement:** Point operations, Histogram modeling, Spatial operations, Transform operations, Multi-spectral image enhancement, False color and pseudo-color, Color Image enhancement. **06 Hrs**
4) **Image Filtering & Restoration:** Image observation models, Inverse & Wiener filtering, Fourier domain filters, Smoothing splines and interpolation, Least squares filters, Generalized inverse, SVD and iterative methods, Maximum entropy restoration, Bayesian methods. **06 Hrs**
5) **Image Analysis & Computer Vision:** Spatial feature extraction, Transform features, Edge detection, Boundary extraction, Boundary representation, Region representation, Moment representation, Structure, Shape features, Texture, Scene matching & detection, Image segmentation, Classification techniques. **06 Hrs**
6) **Image Reconstructions from Projections:** Introduction, Radon transform,

Back projection operator, Projection theorem, Inverse Radon transform, Convolution/ Filter back-projection algorithm. **06 Hrs**

7) **Video Processing:** Fundamental concepts in video – Types of video signals, Analog video, Digital video, Color models in video, Video compression techniques – Motion compensation, Search for motion vectors, H.261, H.263, MPEG I, MPEG 2, MPEG 4, MPEG 7 and beyond, Content based video indexing. **06 Hrs**

Activity beyond Syllabus: Seminar, Simulation based Project.

Reference Books:

1) Anil K. Jain, "Fundamentals of Digital Image Processing," Pearson Education (Asia) Pvt. Ltd., Prentice Hall of India, 2004.

2) Z. Li and M.S. Drew, "Fundamentals of Multimedia",Pearson Education (Asia) Pvt. Ltd., 2004

3) R. C. Gonzalez and R. E. Woods, "Digital Image Processing", 2nd edition, Pearson Education (Asia) Pvt. Ltd, Prentice Hall of India, 2004.

4) M. Tekalp, "Digital Video Processing", Prentice Hall, USA, 1995.

5) K.P.Soman, "Digital Signal & Image Processing', 1st edition, Elsevier India, 2012.

20PDEE354	**Modern DSP**	**(3-0-0) 3**

Contact Hours: 39

Course Learning Objectives (CLOs):

This course focuses on some of the modern techniques in signal processing such as multi rate signal processing, signal transforms and nonlinear filters and adaptive filters.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Analyze and outline** the principles of multirate signal processing techniques	1, 5	-	-
CO-2	**Apply** mathematical concepts of signal transformations.	-	2	6
CO-3	**Determine** system response for different filters given signal / situation.	3, 5	-	6

CO-4	**Analyze** the principles of nonlinear digital filters and **Evaluate** the output of nonlinear digital filters.	1, 4	2	-
CO-5	**Analyze** adaptive filtering techniques and their applications.	4	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	3.0	2.0	3.0	3.0	2.7	1.0

Pre-requisites: Digital Signal Processing

Contents:

1) **Fundamentals of Multirate Systems**: Introduction, Basic Multirate Operations, Interconnection of Building Blocks, The Polyphase Representation, Multistage Implementations, Applications of Multirate Systems. **08 Hrs**
2) **Maximally Decimated Filter Banks:** Introduction, Errors created in the QMF Bank, A Simple Alias Free QMF System, M-Channel Filter Banks, Polyphase Representation, Perfect Reconstruction Systems, Alias Free Filter Banks, Applications. **09 Hrs**
3) **Transforms:** Introduction, Cosine Transform, Sine Transform, Hadamard Transform, Haar Transform, KL Transform. **06 Hrs**
4) **Nonlinear Digital Filtering:** Trimmed Mean Filters, L-Filters, C-Filters, Weighed Median Filters, Ranked-Order and Weighed Order Statistic Filters, Multistage Median Filters, Median Hybrid Filters, Edge-Enhancing Selective Filters, Rank Selection Filters, M-Filters, R-Filters, Nonlinear Mean Filters. **08 Hrs**
5) **Introduction to Adaptive filter:** 3 kinds of estimation, Adaptive filter, Approaches to the development of Linear Adaptive filter, Applications of Adaptive Filters. LMS Adaptive Filters, Overview of the structure & operation of LMS algorithm, LMS algorithm, Summary of the LMS algorithm, Applications of LMS algorithm. RLS Adaptive Filters, exponentially weighted recursive least squares algorithm, selection of the regularization parameter, update recursion for the sum of weighted error squares, example single weight adaptive noise canceller. **08 Hrs**

Reference Books:

1) P.P. Vaidyanathan, "Multirate systems and filter banks" Prentice Hall, 1993.

2) Jaakko Astola, Pauli Kuosmanen, Fundamentals of Nonlinear Digital filtering, CRC Press.

3) Simon Haykin, Adaptive Filter Theory, 4th Edition, Pearson Education.

20PDEE355	Wireless Sensor Networks	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on architecture of Wireless sensor nodes, Operating systems used in WSN, Medium Access Control Protocols, Networks Protocols, Power Management, Time Synchronization, Localization and security issues in WSN.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Identify** various parts of WSN and **explain** their construction and operation	3	-	-
CO-2	**Apply** suitable medium access control technique for a given application of WSN.	3	1	-
CO-3	**Apply** suitable data dissemination and routing protocol for a given application of WSN.	4	5	1
CO-4	**Apply** various techniques and **solve** the problems related to power efficiency and synchronization in WSN.	-	4	1
CO-5	**Apply** the techniques and **determine** solutions various issues related to localization and security issues in WSN	-	5	6

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1.33	-	3	2.4	2	1

Pre-requisites: Sensors and Actuators, Wireless Communication, Microcontrollers, Communication Network protocols.

Contents:

1) **Wireless Sensor Network Basics**: Motivation, Definitions and Background, Challenges and Constraints, Areas of Applications, Node Architecture, Sensing Subsystem, Processor Subsystem, Communication Interfaces, Operating Systems, Functional and Non functional aspects of OS. **05 Hrs**
2) **Medium Access Control:** Medium Access Control, Overview, Wireless MAC Protocols, Characteristics of MAC Protocols in Sensor Networks, Contention-Free MAC protocols, Contention based MAC protocols, Hybrid MAC protocols. **08 Hrs**
3) **Network Layer**: Overview, Routing Metrics, Flooding and Gossiping, Data-centric Routing, Proactive Routing, On-Demand Routing, Hierarchical Routing, Location based Routing, QoS based routing protocols. **08 Hrs**
4) **Power Management and Time Synchronization:** Local Power Management Aspects, Dynamic Power Management, Conceptual Architecture, Clocks and synchronization problem, Time synchronization in WSN, Basics of Time synchronization, Time synchronization protocols. **09 Hrs**
5) **Localization and Security:** Overview, Ranging Techniques, Range based Localization, Range-Free Localization, Event Driven Localization, Fundamentals of Network Security, Challenges of Security in WSN, Security Attacks in Sensor Networks, Protocols and Mechanisms for Security. **09 Hrs**

Reference Books:

1) Waltenegus Dargie, Christian Poellabauer, “Fundamentals of Wireless Sensor Networks”, Wiley Publications, 2014.
2) Kazem Sohraby, Daniel Minoli, Taieb Znati “Wireless Sensor Networks”, Wiley Publications, 2015.
3) Jun Zeng, Abbas Jamalipour "Wireless Sensor Networks", Wiley Publications, 2014.
4) S. Swapnakumar, " A Guide to Wireless Sensor Networks”, Laxmi Publications , 2013.

20PDEE356	Advanced FPGA Design	(3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs): The course focuses on key criteria: area, speed, optimization techniques employed, various system architectures considered in the FPGA method of Design.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1-6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Demonstrate** the basics of FPGA Architecture and its Function mapping.	-	1	2
CO-2	**Understand** Advanced FPGA design principles w.r.t speed and area.	1	2	-
CO-3	**Modeling** of Power and Clock Domain for Digital Circuits.	3	4	2
CO-4	**Design** strategies coding for synthesis.	5	4	3
CO-5	**Design** optimization for Static Timing Analysis.	5	3	4
CO-6	**Analyze** and **explore** the architectural design of FPGA for Deep Learning Applications.	6	5	4

Pre-requisites: Knowledge of FPGA Architecture.

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	2.5	1.33	2	1.5	2.66	3

Contents:

1. **FPGA Design Flow**: Reconfigurable Logic Devices, Design Flow, Field-Programmable Gate Arrays, Basic Architecture, Example Actel Devices: ACT1 logic module, Shannon's expansion theorem, Routing, Programmable I/O Architectures**,** Specialized Function Blocks: Embedded Microprocessors. **5 Hrs**

2. **Architecting Speed & Area**
   Speed: High Throughput, Low Latency, Timing, Add Register Layers, Parallel Structures, Flatten Logic Structures, Register Balancing, Reorder Paths.
   Area: Rolling Up the Pipeline, Control-Based Logic Reuse, Resource Sharing, Impact of Reset on Area, Resources Without Reset, Resources Without Set, Resources Without Asynchronous Reset, Resetting RAM, Utilizing Set/Reset FFPins. **6 Hrs**
3. **Architecting Power:** Clock Control, Clock Skew, Managing Skew, Input Control, Reducing the Voltage Supply, Dual-Edge Triggered Flip-Flops, Modifying Terminations. **Clock Domains:** Crossing Clock Domains, Metastability, Solution 1: Phase Control, Solution 2: Double Flopping, Solution 3: FIFO Structure, Partitioning Synchronizer Blocks, Gated Clocks in ASIC Prototypes, Clocks Module, Gating Removal. **6 Hrs**
4. **Coding for Synthesis:** Decision Trees, Priority Versus Parallel, Full Conditions, Multiple Control Branches, Traps, Blocking Versus Nonblocking, For-Loops, Combinatorial Loops, Inferred Latches, Design Organization, Partitioning, Data Path Versus Control, Clock and Reset Structures, Multiple Instantiations**.** **6 Hrs**
5. **Synthesis Optimization:** Speed Versus Area, Resource Sharing, Pipelining, Retiming, and Register Balancing, The Effect of Reset on Register Balancing, Resynchronization Registers, FSM Compilation: Removal of Unreachable States**.** **6 Hrs**
6. **Static Timing Analysis:** Standard Analysis, Latches, Asynchronous Circuits, Combinational Feedback**.** **4 Hrs**
7. **Accelerating the CNN Inference on FPGAs :** Introduction, Background on CNNs and Their Computational Workload, General Overiew, Inference versus Training, Inference, Layers, and CNN Models, FPGA-Based Deep Learning Computational Transforms: Winograd Transform and Fast Fourier Transform, Loop Unrolling. Loop Tiling. **6 Hrs**

Activity Beyond Syllabus: Seminar on Reconfigurable Computing.

Reference Books:

1) Steve Kilts, Advanced FPGA Design Architecture, Implementation and Optimization, Wiley Inter-science, 2007.
2) M. Gokhale, P. Graham, Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays, Springer, 2005.
3) Mahmoud Hassaballah, Ali Ismail Awad, Deep Learning inComputer Vision, CRC Press, Taylor & Francis Group,2020.

4) Ian Goodfellow, Yoshua Bengio, Aaron Courville, Deep Learning, MIT Press. https://www.deeplearningbook.org/

20PDEE357 MEMS (3-0-0) 3

Contact Hours: 39

Course Learning Objectives (CLOs):

The course focuses on the study of various electromechanical sensors, actuators and their transduction principles at micro and nanoscale. The course covers the advanced domains of electronics, material science and mechanics at research level.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to:		**Mapping to POs(1 to 6)**		
		Substantial Level (3)	**Moderate Level (2)**	**Slight Level (1)**
CO-1	**Understand** and appreciate the significance of MEMS, as an emerging area in the field of electronics.	-	3	6
CO-2	**Identify** various micro sensors and actuators being used for electromechanical applications.	4	-	-
CO-3	**Discuss** the processes involved in the fabrication of different micro sensors and micro actuators.	4	-	-
CO-4	**Design** simple micro sensors and actuators using CAD softwares and perform simulations.	-	-	1
CO-5	**Classify** various micro system packaging technologies related to MEMS.	-	5	-
CO-6	**Apply** processing steps, scaling laws and transduction principles towards the realization of MEMS product design.	4	5	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping Level	1	-	2	3	2	1

Pre-requisites: Physics, Electronics, Engineering Mathematics, Material Science, Basic Mechanical principles

Contents:

1) **Overview of MEMS & Microsystems**: MEMS & Microsystems, Typical MEMS and Micro system products — features of MEMS, The multidisciplinary nature of Applications of Microsystems.
   Scaling Laws in Miniaturization: Introduction to scaling, scaling in geometry, scaling in rigid body dynamics, scaling electrostatic forces, electromagnetic forces and electricity. **8 Hrs**
2) **Transduction Principles in MEMS & Microsystems:** Electromechanical Transducers: Piezoelectric, Electrostrictive, Magnetostrictive transducers, Electrostatic, Electromagnetic, Electrothermal actuators.
   Microsensing for MEMS: Piezoresistive, Capacitive, Piezoelectric, Resonant, SAW sensors, Bio-MEMS and Biosensors. Micro-accelerometers, Micro-gyroscopes. **10 Hrs**
3) **MEMS materials and Fabrication Techniques:** Materials used for MEMS, Photolithography, Ion-implantation, diffusion, oxidation, CVD, PVD, etching techniques. Some MEMS fabrication processes: Surface micro-machining, Bulk micromachining, LIGA process. **8 Hrs**
4) **Micro System Design and Modeling:** Introduction, Design considerations: Process design, Mechanical design, Modeling using CAD tools: Multiphysics or Intellisuite or MEMS CAD, Features and Design considerations of RF MEMS, MEMS switches, MEMS inductors and capacitors, Design and Modeling: case studies - i) Cantilever beam ii) Micro switches. **8 Hrs**
5) **Micro system packaging:** Over view of mechanical packaging of micro electronics micro system packaging, Interfaces in micro system packaging, Packaging technologies. **5 Hrs**

Reference Books:

1) Tai Ran Hsu, “MEMS and Micro Systems: Design and Manufacture”, Tata McGraw Hill, 2002.
2) V.K.Varadan, K.J.Vinoy, K.A.Jose, “RF MEMS and their Applications”, Wiley-India, 2011.
3) Boca Raton, “MEMS and NEMS: Systems, Devices and Structures”, CRC Press, 2002.

4) J. W. Gardner and V. K. Vardan, "Micro Sensors MEMS and SMART Devices", John Wiley, 2002 N. Maluf, "Introduction to Micro Mechanical Systems Engineering, Artech House", Norwood, MA, 2000.

20PDEL300 Internship (4 weeks) 3

Course Learning Objectives (CLOs):

The curriculum has the support for internship to be carried out during vacation immediately after the completion of II semester examination for a minimum period of four weeks in any of the reputed Industries/ Academic Institutes/ R&D Organizations. Students may identify the Industries considering their career choice. The objectives are:

- Internships are intended to provide students with an opportunity to apply theoretical concepts from the classroom to the realities of the field.
- Will expose students to the industrial environment, which cannot be simulated in the classroom and hence creating competent professionals for the industry.
- Provide possible opportunities to learn understand and sharpen the real time technical / managerial skills required at the job.
- Provides exposure to the current technological developments relevant to the subject area of training.
- Provides an opportunity to explore and develop their careers through professional practice. Helps students to communicate in a workplace environment in a clear and confident manner and articulate their experience and skills to potential employers.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Acquire** practical experience in an organizational setting	-	1,6	-
CO-2	**Apply** the knowledge and skill set in engineering design processes appropriate to the internship program.	1,4	3,5	-
CO-3	**Apply** modern tools and processes to solve the live problems.	-	4	-
CO-4	**Get** an opportunity to learn new	-	5	-

	skills			
CO-5	**Learn** strategies like time management, multi-tasking, communication and team work skills in an industrial setup.	-	2,5,6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	2.5	2	2	2.5	2	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field and explore solutions. They are required to know the functions of engineers in managing the floor. Current technological developments, organizational behavior, time management, professional ethics, etc. need to be understood.

2) The above skills obtained need to be documented and presented.

Reference Material:

1) Technical references/research papers
2) Manuals
3) Software packages

20PDEL301 Project Phase - I (0-0-15) 9

Contact Hours:100

Course Learning Objectives(CLOs):

The course focuses to encourage innovation, enhance research culture and promote independent learning. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes(COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Identify** innovative/research based problem statement through literature survey	1,4,5	-	-

CO-2	**Explore** and **analyze** possible technical solutions for the problem identified	4,5	-	-
CO-3	**Demonstrate** the work progress	3	-	-
CO-4	**Prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in the previous semesters.

Contents:

1) The students are expected to know the current challenges in the relevant field through literature survey and select a topic from emerging area relevant to the branch.

2) The students are expected to explore and analyze all possible technical solutions for the problem identified and start working on the same using tools. Preliminary design, analysis, simulation etc. is to be done in this phase.

3) The students are expected to document the work done in a systematic way and learn/improve the presentation skills.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools

IV semester

20PDEL400 Project Phase - II (0-0-20)22

Contact Hours: 200

Course Learning Objectives (CLOs):

The course focuses to encourage innovation, enhance research culture and promote team work. It also promotes for attaining leadership qualities with ethical values in developing and applying technology for the betterment of society.

Course Outcomes (COs):

Description of the Course Outcome: At the end of the course the student will be able to		**Mapping to POs (1-6)**		
		Level 3 Substantial	**Level 2 Moderate**	**Level 1 Slight**
CO-1	**Design** and **Implement** the solution	1,4,5	-	-
CO-2	**Discuss** the outcome of the work	3,4,5	-	-
CO-3	**Justify** the approach and **Integrate** the work carried out by producing technical paper	2,3	-	-
CO-4	**Organize** the topics in a systematic manner and **prepare** the report in a specific format	2	6	-
CO-5	**Present** the work in a systematic way imbibing professional ethics	2	6	-

POs	PO1	PO2	PO3	PO4	PO5	PO6
Mapping levels	3	3	3	3	3	2

Pre-requisites: Knowledge of theory and practical courses learnt in previous semesters.

Contents:

1) The students are expected to continue the work providing feasible solutions, justify the approach, defend the same and present the work in national / international conferences or journals.

1) The students are expected to document the work done in a systematic way and deliver the oral presentation.

Reference Material:

1) Reputed Journals

2) Engineering books, Manuals

3) Software tools